REMARKS

Claims 1 and 3 to 45 are pending in this application of which claims 1, 27, 34, 38, 42 and 44 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

The Examiner has objected to claims 9, 43 and 45. Based on the foregoing claim amendments, Applicants respectfully request withdrawal of the claim objections.

Claims 1, 3 to 16, 19 to 32 and 34 to 45 were rejected under 35 U.S.C. 102(e) as being anticipated by Brinkerhoff et al. (U.S. Patent Publication Number 2004/0213255 hereinafter "Brinkerhoff")

Previously presented claim 1 is directed to a processor. The processor includes a first multi-threaded processor engine configured for connection to a serial link, a second multi-threaded processor engine, coupled to the first multi-threaded processor engine by an interface, to process data received by the first multi-threaded processor over the serial link and to provide the processed data to the first multi-threaded processor engine for transmission over the serial link and one or more communication data structures usable by the first and second multi-threaded processor engines to control interaction therebetween. At least one of the one or more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1. In particular, Brinkerhoff does not disclose or suggest that at least one of the one or

more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine (emphasis added).

The Examiner has stated that a first multithreaded processor engine is a line card processor 74 and a second multithreaded processor engine is a CPU 62A having processors 63 (see page 3 of the Office Action). The Examiner has failed to provide support in Brinkerhoff that line card processor 74 is a multithreaded processor. Furthermore, the Examiner has not addressed Applicants' arguments with respect to CPU 62A being a multithreaded processor. The Examiner had indicated in the first office action that Brinkerhoff indicates that CPU 62A is a MIPS (see page 4 of Office Action dated June 11, 2007). Applicants had requested that the Examiner provide support that a MIPS is a multithreaded processor, but the present office action provides no support that either processor 74 and CPU 62A are multithreaded processors. If the Examiner is suggesting that a multithreaded processor is inherent in MIPS, Applicants respectfully request that the Examiner provide support (See MPEP §2112 Section IV). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic (see In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); In re Oelrich, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981)). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of

circumstances is not sufficient' " (emphasis added, see In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)). Applicants respectfully submit that a MIPS does not necessarily mean a multithreaded engine.

Also, the Examiner has erroneously indicated that the line card processor 74 uses the scheduler 806. Brinkerhoff states that system 800 is a specific embodiment of CPU 62a (see paragraph [0102]. However, the Examiner statements with respect to processor 816 in system 800 are inconsistent with what Brinkerhoff teaches. Put simply, processor 816 is not a line card processor 74, and thus, line card processor does not use system 800. Thus, Brinkerhoff never discloses or suggests that the processor 62A and processor 74 use the scheduler 804 to control the rate at which the processed data is provided to the processor 74 by the processor 62A. Therefore, Brinkerhoff does not disclose or suggest that at least one of the one or more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine.

Independent claims 27, 34 and 38 include the feature that at least one of the one or more communication data structures is usable by the first and second multi-threaded processor engines to control the rate at which the processed data is provided to the first multi-threaded processor engine by the second multi-threaded engine. Applicants submit the Brinkerhoff reference should also be withdrawn with respect to claims 27, 34, and 38 for at least the same reasons as claim 1.

Furthermore, the applied art is not understood to disclose or suggest other features of claim 27, 34, and 38. In particular, Brinkerhoff does not disclose or suggest that the at least one

or more communication data structures includes a shared memory including memory locations corresponding to each of the channels that handles cell data and that each memory location stores a count value indicating the number of cells transmitted by the first multi-threaded processor engine for the channel to which such memory location corresponds (emphasis added).

The Examiner has indicated that the line card 70 stores line rate information that is accessed by the CPU 62a (see page 10 of the Office Action). Applicants respectfully point out that "line rate information" is not "a count value indicating the number of cells transmitted by the first multi-threaded processor." The line rate information only teaches what each line card is capable of transmitting over time not what has actually been "transmitted." The Examiner has indicated that a parameter T may represent the number of ATM cells which have been transmitted over line 309 in FIG. 3A (page 11 of the Office Action). Applicants finds this confusing and question its relevancy. First, the parameter T is not stored on the line cards 70. Second, the line 309 is not the output of the line cards 70. Therefore, Brinkerhoff does not disclose or suggest that the at least one or more communication data structures includes a shared memory including memory locations corresponding to each of the channels that handles cell data and that each memory location stores a count value indicating the number of cells transmitted by the first multi-threaded processor engine for the channel to which such memory location corresponds.

Moreover, the applied art is not understood to disclose or suggest still other features of claims 27, 34, and 38. In particular, Brinkerhoff does not disclose or suggest that the second multi-threaded processor engine, after polling one of the memory locations of a selected one of

the channels, is operable to compare the count value with another count value indicative of a number of cells scheduled for transmission and maintained by the second multi-threaded processor engine, to determine a number of cells in flight (emphasis added).

Applicants note that the Examiner has not addressed this limitation. Specifically, the Examiner has not shown another count value indicative of a number of cells scheduled for transmission.

Applicants submit that independent claim 42 includes corresponding features to claims 27, 34, and 38. Applicants submit that the Brinkerhoff reference should be withdrawn with respect to claim 42 for at least the same reasons as claims 27, 34 and 38.

Independent claim 44 is directed to a computer-readable medium having stored thereon instructions that when executed by a machine result in the following enabling multi-threaded packet processing of data received from a communications medium via a multi-threaded physical layer network processor engine, which receives serial data from a serial link, or other media device; and using the multi-threaded physical layer network processor engine as a co-processor to perform a hardware accelerator task associated with the multi-threaded packed processing.

The applied art is not understood to disclose or to suggest the foregoing features of claim 44. In particular, Brinkerhoff does not disclose or suggest using the multi-threaded physical layer network processor engine as a co-processor to perform a hardware accelerator task associated with the multi-threaded packed processing.

The Examiner states that "co-processor 74 performs hardware accelerator task such as data parcel switching, media control management, framing, interworking, protocol conversion,

data parsing, etc. (para. 91)" (see page 11 of the Office Action). Applicants respectfully point out that the statement by the Examiner is in error. Paragraph [0091] of Brinkerhoff refers to the interface 68 and not the co-processor 74. In fact, the co-processor 74 is not even referenced in Paragraph [0091] of Brinkerhoff. Therefore, Brinkerhoff does not disclose or suggest using the multi-threaded physical layer network processor engine as a co-processor to perform a hardware accelerator task associated with the multi-threaded packed processing.

For at least the foregoing reasons, Applicants request withdrawal of the art rejections.

Applicants submit that all dependent claims now depend on allowable independent claims.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for withdrawing the prior art cited with regards to any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicants submit that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the address below. Applicants' attorney can be reached by telephone at (781) 401-9988 ext. 123.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 50-0845 referencing Attorney Docket: INTEL-008PUS.

Respectfully submitted,

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